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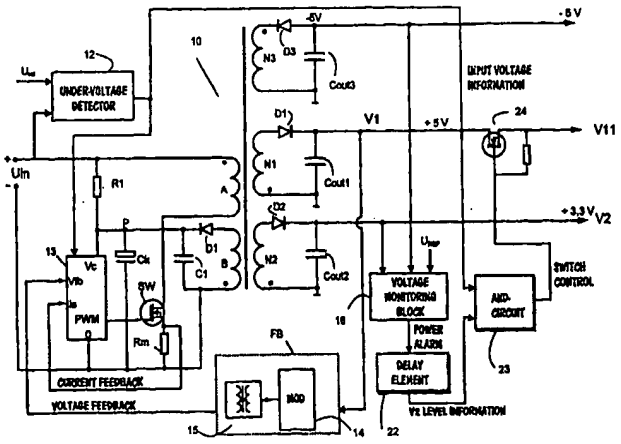

(57) Abstract

The switched mode power supply according to the invention has an input voltage under–voltage indicator (12), an output voltage monitoring block (16), a circuit (23) performing a logical function and a controlled switch (24). The circuit performing a logical function functions in such a way that it controls the controlled switch (24) to close at once when the first output voltage monitoriing circuit has found that this voltage has reached its nominal value and input voltage information indicates that there is a sufficient voltage in the switched mode power supply primary. The load supplied by the switched mode power supply will hereby first be provided in a controlled manner with a first voltage (V1) and only thereafter with a second voltage (V2). If the input voltage is cutt off or it becomes too low, the circuit performing a logical function will control the switch (24) to open at once, whereby the first voltage (V1) is switched off the load. On the other hand, energy charged in capacitors of the switched mode power supply secondary circuit will keep the second voltage (V2) at its nominal value for some time. In this way, the first voltage (V1) is first switched off the load in a controlled manner and the second voltage falling according to a time constant will remain effective for some time.

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DC-DC CONVERTER

Field of the invention

This invention concerns a DC-DC converter. An advantageous application of a system according to the invention is telecommunications equipment having several parallel board units, each one of which needs a power supply of its own.

Background of the invention

Switched-mode power supplies have an increasing share in power supply design. This is due to many advantages of these, such as a good coefficient of efficiency, a broad input voltage range and the possibility to make compact and light-weight power supplies.

Nowadays, fly-back topology is used more and more often in switched-mode power supplies. Topology means that circuit configuration which determines how power will be forwarded in the power supply. The major advantage of a power supply of the fly-back type is its simple and cheap structure, which is suitable for use also in multiple output power supplies.

In the switched-mode power supply the relation of ON and OFF cycles of the primary circuit switch is controlled with the aid of pulse width modulation (PWM). The PWM control circuit which controls the switch may be located in the power supply either on the primary side or on the secondary side depending on which characteristics are important in each case. The solution will be described more closely in the following.

Figure 1 shows the fundamental interface of the known fly-back switched-mode power supply known as such when the PWM control circuit is located on the primary side. The power supply comprises in a known manner, firstly, a converter 10, through which power is transferred from the primary side to the secondary side, a switch SW in the primary circuit which may be e.g. a power MOSFET as shown in the figure or a bipolar transistor. The primary current passing through primary coil A is cut off with the switch. In addition, the power supply comprises a PWM control circuit 13 which controls the switch and which by controlling the duty cycles of the switch controls the output voltages, which in this example are +5 V, -5V and +3.3 V respectively. The control takes place with the aid of pulse width modulation

(PWM), that is, by controlling the relation of ON and OFF cycle lengths of the switch.

The PWM control circuit 13 controlling the switch pulse width may function either in the so-called voltage mode based on the output voltage or in the so-called current mode based on the primary current and output voltage. A majority (80 %) of modern fly-back switched-mode power supplies use current mode circuits, because it is easier to design a controller operating in the current mode. For this reason, the example in Figure 1 shows a control circuit which is a control circuit 13 working in the current mode and which performs its control function based on output voltage information about switched mode power supply received from feedback circuit FB and on current information received from switch SW.

The voltage information is formed here by taking a sample of the +5 V output voltage to an amplitude modulator circuit. The output signal of the amplitude modulator circuit is connected through a galvanic de-coupling converter 15 or opto-coupler to voltage feedback input VFb of control circuit 13. The current information is obtained from switch SW with current measuring resistance Rm by taking a sample of the voltage affecting over the resistance to current measuring input Is of control circuit 13. Control circuits are commercially available from different manufacturers.

On the primary side of the power supply there is also a separate auxiliary voltage coil B, which is used for forming an operating voltage for control circuit 13. Between the poles of the auxiliary voltage coil there is a rectifier diode D1 and a capacitor C1 in series over which the operating voltage is formed. Resistance R1 is a charging resistance for starting capacitor Ck.

In this example there are three secondary coils indicated by reference symbols N1, N2 and N3 in the secondary circuit of the power supply. One pole of secondary coil N1 is connected to earth and rectifier diode D1 and output capacitor Cout1 are connected in series between this pole and the other pole of the coil. Correspondingly, one pole of secondary coil N2 is connected to earth and rectifier diode D2 and output capacitor Cout2 are connected in series between this pole and the other pole of the coil. Secondary coil N3 and rectifier diode D3 are connected similarly, but the winding and diode have another direction, because the output voltage is negative.

In most cases, power supplies also contain an under-voltage indicator for the primary side and monitoring of output voltages. The under-voltage indicator 12 compares the input voltage Uin of the switched mode power supply with a reference voltage U_{ref} and when the input voltage becomes too low indicator 12 will give an alarm signal to control circuit 13. The indicator may simply be a comparator. The voltage monitoring circuit 16 on the output side compares output voltages, here +3.3 V and -5 V voltages, with reference voltages, and when voltages differ from established values the monitor will give an alarm signal POWER ALARM to the control circuit.

Starting of a power supply according to Figure 1 takes place in the following manner. Starting capacitor Ck is charged through current-limiting charging resistance R1 until the voltage occurring at the operating voltage input Vc of the control circuit becomes so high that control circuit 13 begins giving control pulses to switch SW. As a result of this, the power supply will start and a voltage is brought about in auxiliary voltage coil B which is rectified by diode D1 and which is used for forming the control circuit's operating voltage and the control power for the switch.

The output voltages of a switched-mode power supply of the kind described will achieve their final values after starting in the secondary circuit of converter 10, at the rate of time constants determined by capacitors Cout1,...,Cout3 of the output voltage circuits and by the load. Since the load and capacitance values of the secondary circuit are of different magnitude, the output voltages will achieve their nominal values at different times. Of course, the matters described above are also valid in reverse, when the switched mode power supply is turned off. Each output voltage will drop at the rate determined by the time constant of its current circuit, and it is almost impossible to say beforehand in which order voltages will drop to zero.

It is normally of no significance in what order the output voltages of a switched-mode power supply will achieve their output values after starting and achieve zero value after being turned off. There are applications, however, where the exact order of voltage increase and decrease is an extremely important matter.

Such applications are Application-Specific Integrated Circuits (ASIC), where several operating voltages occur at different levels. They must be turned on and off in an exactly determined order. If this is not done, the circuit may be destroyed.

It is a problem that in known switched-mode power supplies there are no mechanisms allowing a desired switching order of output voltages, but the matter must be handled with separate switching circuits outside the power supply. This is a troublesome method which increases costs.

It is hence an objective of the present invention to bring about a switched-mode power supply which eliminates the said problem. The power supply is characterised by the definitions in the independent claims.

Brief summary of the invention

The invention utilises functional blocks already existing in known switched mode power supplies, such as an output voltage monitoring block on the secondary side and an under-voltage indicator on the primary side. The invention is especially based on the idea of also using the fact besides known blocks that different time constants of circuits on the switched mode power supply's secondary side cause a slowing down effect on the increase and decrease rates of output voltages.

The switched-mode power supply according to the invention has at least one output voltage monitoring block, a circuit performing a logical function and a controlled switch. An existing block is used as the output voltage monitoring block, if there is such a block in the switched mode power supply.

The output voltage monitoring block is connected on its input side to at least one output voltage and on its output side the monitoring block is connected functionally to one input of a circuit performing a logical function. After the monitored output voltage, which is here called the second output voltage, has achieved its nominal value, the state is changed of the monitoring block output and thus also the state of the circuit performing the logical function.

Such input voltage information is conducted to the second input of the circuit performing the logical function which states whether the switched mode power supply input voltage is acceptable or too low for an acceptable switched mode power supply operation. The input voltage information is obtained directly from the primary under-voltage indicator, if the switched mode power supply already has one.

The controlled switch will switch the first output voltage of the switched mode power supply circuit to the load or off the load according to the control.

The function of the circuit performing a logical function is such that it controls the controlled switch to close at once when the second output voltage monitoring circuit has found that this voltage has achieved its nominal value and when the input voltage information indicates a sufficient input voltage for the switched mode power supply. The load supplied by the switched mode power supply will hereby have controlled use first of the second output voltage and only thereafter of the first output voltage.

If the switched mode power supply input voltage is cut off or it becomes too low, the input voltage information will indicate that the input voltage of the switched mode power supply has dropped below the acceptable value. As a result of this, the output of the circuit performing a logical function will change into a state which controls the switch to open, whereby a first output voltage will be switched off the load. On the other hand, the energy charged in capacitors of the switched mode power supply's secondary circuit will keep the second output voltage at its nominal value for some time, from which the voltage will fall to zero value in a manner determined by the time constant. Thus, the first output voltage is first switched off the load in a controlled manner and the second output voltage falling according to the time constant will remain effective for some time.

If for some reason the second output voltage falls below the nominal value, the circuit performing the logical function will control the controlled switch to open, thus immediately switching the first output voltage off the load. The second output voltage falling according to the time constant will remain effective for some time.

List of figures

The invention will be described in greater detail with the aid of the attached diagrammatic figures, wherein:

Figure 1 shows a known fly-back switched mode power supply;
Figure 2 shows an interface according to the invention;
Figure 3 shows the interface applied to the switched mode power supply in Figure 1;

Figures 4A-4E show events when the switched mode power supply is started;

Figure 5 shows a possible embodiment; and

Figures 6A-6D show events when the input voltage disappears.

Description of the preferred embodiment of the invention

Figure 2 shows the essential parts of the interface according to the invention. The order in which switched mode power supply output voltages V1 and V2 are connected to the load, which is an ASIC circuit in this example, must be such that when the switched mode power supply is switched on and off voltage V2 must be switched to the load before voltage V1 and voltage V1 must be switched off the load before voltage V2 independently of the current level of output voltages.

The interface comprises a switched mode power supply output voltage monitoring block 21, a circuit 23 performing a logical function and a controlled switch 24. In addition, it is advantageous to use a delay element 22. The circuit performing a logical function carries out an AND operation in this example. Inputs of circuit 23 are input voltage information stating whether the switched mode power supply input voltage is acceptable or not, and information given by voltage monitoring block 21 stating whether output voltage V2 is acceptable or not. If both inputs state that the voltages are acceptable, AND circuit 23 will provide a control which controls switch 24 to close, whereby the switched mode power supply output voltage V1 is switched to the load. If both inputs or only one input of the AND circuit state that the checked voltage is not acceptable, AND circuit 23 will control switch 24 to open, whereby the switched mode power supply secondary voltage V1 will not affect the load. The second switched mode power supply output voltage V2 affects the load all the time.

Since known switched mode power supplies in many cases already have an output voltage monitoring block located on the secondary side, block 16 in Figure 1, and an input under-voltage indicator located on the primary side, block 12 in Figure 1, these may be utilised and the output of one may be conducted directly and the output of the other by way of delay element 22 as inputs for AND circuit 23.

According to Figure 2, the voltage V11 affecting the load and the ASIC circuit is either zero or a full nominal voltage V1 depending on the

position of switch 24, and any change between these states is in steps. On the other hand, the switched mode power supply output voltage V2 affects the load all the time, so depending on capacitors of the switched mode power supply's secondary circuit, e.g. Cout2 in Figure 1, any change in the nominal voltage to zero is not in steps but will follow a curve determined by the time constant of the concerned secondary circuit RC. This fact is of great importance to the arrangement according to the invention, as will be indicated later.

Figure 3 shows a known switched mode power supply in accordance with Figure 1 supplemented with the elements according to the invention which are shown in Figure 2. The output voltage V2 produced by the switched mode power supply is 3.3 V and the output voltage V1 is +5 V. These voltages are operating voltages of the ASIC circuit which is the load (not shown). Due to the nature of the load, the 3.3 V operating voltage must always be switched to the load before the 5V operating voltage and, correspondingly, when the voltages are separated from the load, the 5 V voltage must be separated first and the 3.3 V voltage only thereafter.

Events when starting the switched mode power supply will be described referring to Figure 3 and to Figures 4A-4E. When input voltage Uin is switched on to the switched mode power supply, the primary capacitors (not shown in the figure) will begin getting charged and thus the voltage of primary coil B will rise, Figure 4A. After a certain time the alarm limit of under-voltage indicator 12 is exceeded and its output voltage rises, indicating that the input voltage is sufficient, Figure 4B. The input voltage information is conducted to the input of AND circuit 23. A voltage is induced in the auxiliary voltage coil of the switched mode power supply, so the pulse width modulator will have an operating voltage. The switched mode power supply then starts to operate.

Capacitors Cout1,...,Cout2 on the output side begin getting charged and secondary output voltages increase. Output voltage V2 affects the load directly and increases beginning from zero towards the nominal voltage of 3.3 V, Figure 4C. Voltage monitoring block 16 compares voltage V2 with the reference voltage, which is e.g. 3 V. When V2 is lower than the reference, the block will give a power alarm signal, that is, the output voltage of the block is low. When voltage V2 bypasses the reference signal, the voltage of the power alarm signal will rise, Figure 4D. This is seen after a

short time ΔT determined by delay element 22 in the second input of AND circuit 23. The circuit now notices that both inputs are up and it gives a positive control voltage to the FET transistor 24 gate functioning as a switch. FET hereby becomes conductive and switches the +5 V voltage V1 to the load, Figure 4E. Thus the load first receives voltage V2 (3.3 V) and only then voltage V1 (+5 V) after the time ΔT determined by the delay element.

The excellency of the arrangement according to the invention is seen in how it works when the input voltage Uin of the switched mode power supply drops. This is described in the following, still referring to Figure 3 and also to Figures 6A-6D.

When input voltage Uin falls below the established alarm limit, Figure 6A, the state of the under-voltage indicator input changes, that is, the output voltage drops, Figure 6B. This is seen immediately in the corresponding output of AND circuit 23, in consequence of which the circuit controls switch 24 to a closed state and the 5 V voltage V1 disappears from the load, Figure 6C. The fall of input voltage Uin has at the same time caused turning off of the switched mode power supply. But the 3.3 V voltage V2 does not disappear at once, because energy charged in capacitors Cout2 of the secondary voltage circuit keeps the voltage at 3.3 V for some time, from which it will then fall by and by as the capacitors discharge, Figure 6D. The discharge time is marked as ΔT1 in the figure.

Those events will also be described which occur when the 3.3 V output voltage V2 falls below the acceptable limit due to a short circuit or overload. The state of the output voltage of the voltage monitoring block 16, which compares voltage V2 with a reference value, changes, that is, falls at once when V2<Uref. This is seen in the state of the corresponding input of AND circuit 23 which also falls. As a result, the circuit input closes switch 24 thus turning off the 5 V voltage V1 from the load before the 3.3 V voltage V2 has time to fall too low.

Such a case will finally be examined where the 5 V output voltage V11 is short circuited. The short circuit causes an increase in the switched mode power supply primary current, so the voltage affecting over the current measuring resistance Rm of the primary circuit will increase. An internal over-current protection turns off the switched mode power supply. Output voltages V1 and V2 start falling, but switch 24 separates the +5 V voltage V1 from the load before the 3.3 V voltage V2 falls too low. After a moment the

switched mode power supply tries to restart and if there is still a short circuit on the secondary side, the series of events presented above will be repeated. During a short circuit average currents are so small in the switched mode power supply that the switched mode power supply will not be destroyed.

Figure 5 shows a possibility of embodying the interface according to the invention. The figure shows secondary circuits of the switched mode power supply in Figure 3 and the reference numbers are the same in applicable parts. Circuit 23 carrying out the AND logical function is here implemented with three transistors: with a transistor 31 working as a switch and controlling the actual transistor 24 working as a switch and with a first transistor 322 and a second transistor 33 which are located in the base circuit of transistor 31 and which are connected in series. These two transistors thus control transistor 31 which functions as a switch. To separate the primary circuit and the secondary circuit electrically from each other, input voltage information is brought to opto-coupler 32, to which belongs a first transistor 322 which will become conductive when a positive input voltage affects diode 321, that is, information that the input voltage is okay. Transistor 31 connects a control voltage to the gate of switch 24 when it receives control itself to the base. Transistor 31 receives an emitter voltage from step-up circuit 34, which steps up the +5 V voltage to a +12 V voltage. Implementation of the step-up circuit is well known.

For transistor 31 to become conductive to close switch 24, its base circuit transistors 322 and 33 must be in a conductive state at the same time. Logically, this corresponds to the AND function. The first transistor 322 is in a conductive state at once when the input voltage is acceptable. The second FET transistor 33 becomes conductive when a positive control voltage is brought to its gate. This will take place when the voltage monitoring block 16 has found that voltage V2 is acceptable. The gate voltage will not change at once, however, but after a brief delay ΔT caused by an RC connection, resistance 222 and capacitor 223, functioning as a delay element. When both base circuit transistors are conductive, switch 24 will connect voltage V1 to the load.

When either input signal, "input voltage information" and "power alarm", changes into the other state, thus making known that the input voltage or output voltage V2 of the switched mode power supply has

dropped too much, the base circuit of transistor 31 will be cut off and this causes transistor 24 to become non-conductive, whereby voltage V1 will disappear from the load.

There is a diode in parallel with the RC link 222, 223 functioning as delay element for the reason that the gate voltage of FET transistor 33 will be allowed to discharge this way if the output signal of voltage monitoring block 14 drops due to a drop in voltage V2 caused by the load or a short circuit.

Although the invention has been described above referring to examples in the attached drawings, it is obvious that the invention is not limited to these, but it may be modified in accordance with the definitions of the claims. Implementation at circuit level may be done in many different ways. The interface performing a logical function need by no means be an AND circuit. Depending on the switched mode power supply interface and voltage polarity, other interfaces performing a logical function may also be used. Suitable interfaces are OR (output logical "0" only when both inputs are in the state of logical "0"), NOR (output is output is logical "1" only when both inputs are in a state of logical "0") and NAND (output is output is logical "0" only when both inputs are in a state of logical "1").

Even the order of voltage switching may be another one than the one presented above. The switched-mode power supply need not be of the fly-back type, but some other power supply will do. If the power supply does not already have such voltage monitoring of the input and output sides which is required by the interface of the invention, such must be connected to the power supply.

Claims

1. A switched mode power supply comprising

- a converter (10) provided with primary and secondary coils (N, N1, N2), for forming at least a first (V1) output voltage and at least a second output voltage (V2),

- in a primary circuit an under-voltage indicator (12), the input of which is affected by an input voltage and from the output of which input voltage information is obtained which states whether the input voltage is above or below a pre-established alarm limit,

- in a secondary circuit a voltage monitoring block (16), one input of which is affected by a second output voltage (V2) and from the output of which level information is obtained which states whether the second output voltage is above or below a pre-established monitoring limit,

c h a r a c t e r i z e d in that the power supply also comprises:

- a circuit (23) performing a logical function, one input of which is functionally connected to the output of an under-voltage indicator (12) and the other input of which is functionally connected to the output of a voltage monitoring block (16) and from the output of which a control signal is obtained which has a first value only when the input voltage is above a pre-established alarm limit and the second output voltage (V2) is above a pre-established monitoring limit,

- a controlled switch (24), which in response to the first value of a supplied control signal will connect a first output voltage (V1) with a first output terminal of the switched mode power supply and in response to a second value of the control signal will separate the first output voltage (V1) from the first output terminal of the switched mode power supply.

2. A Switched mode power supply as defined in claim 1,

c h a r a c t e r i z e d in that the circuit carrying out the logical function comprises

a transistor (31) functioning as a switch supplying a control signal to the controlled switch (24),

a first transistor (322) and a second transistor (33) connected in series on the base of a transistor (31) functioning as a switch so that input voltage information is conducted functionally to the base of the first transistor and a level information signal is conducted functionally to the base of the second transistor (33), whereby when the input voltage is above a pre-

established alarm limit and the second output voltage (V2) is above a pre-established monitoring limit both the first transistor and the second transistor and thus the transistor (31) functioning as a switch will change into a conductive state.

3. Switched mode power supply as defined in claim 2, c h a r a c t e r i z e d in that the first transistor is part of an opto-coupler (32), the input of which is functionally connected to the output of an under-voltage indicator (12), whereby a signal providing input voltage information is separated galvanically from the first transistor.

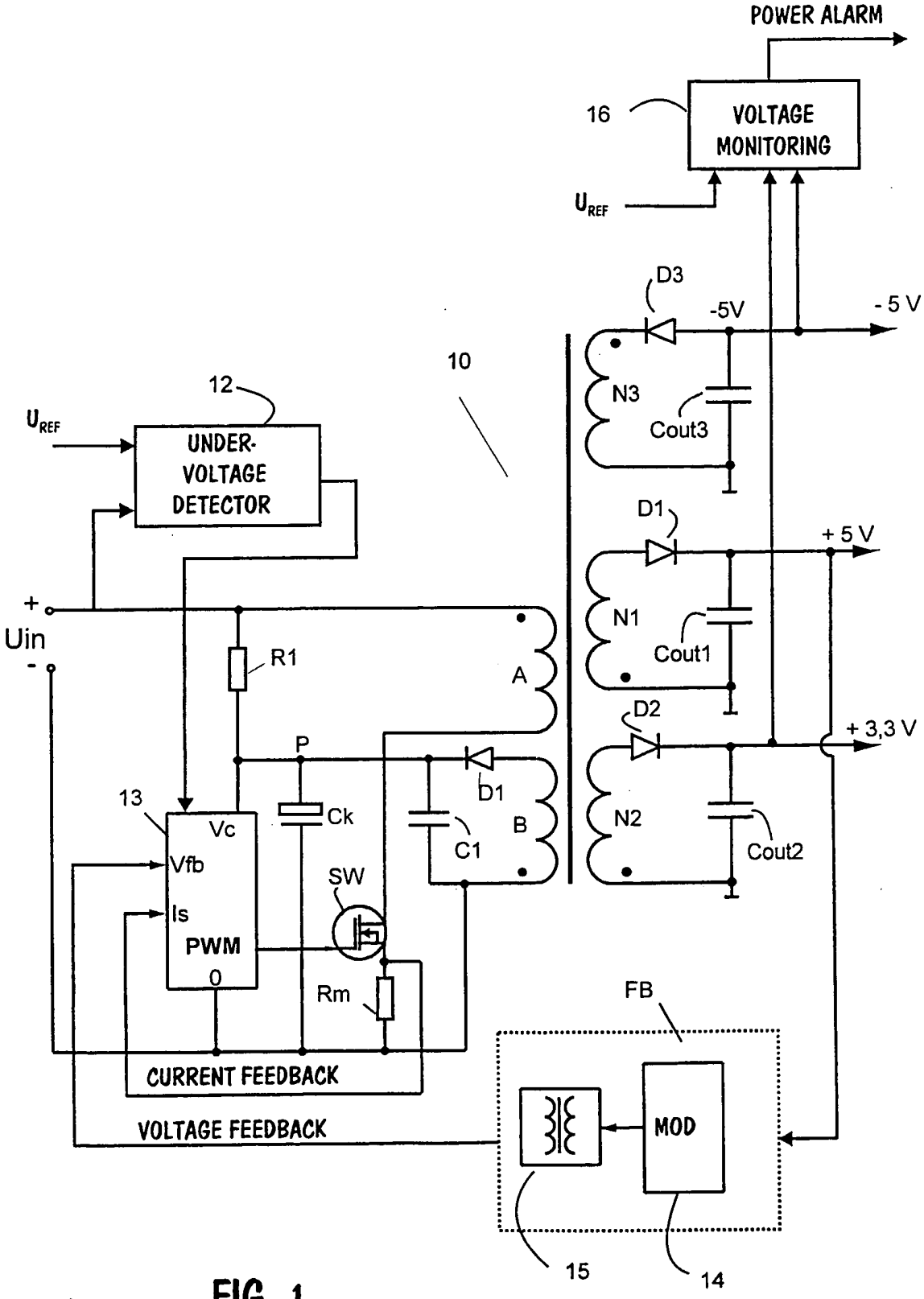
4. Switched mode power supply as defined in claim 1, c h a r a c t e r i z e d in that it has a delay element (22) connected between the voltage monitoring block (16) and the circuit performing a logical function, whereby any change in the level information signal is seen delayed in functions of the circuit performing a logical function.

5. Switched mode power supply as defined in claim 2, c h a r a c t e r i z e d in that it has a delay element (22) connected between a second transistor (33) and a voltage monitoring block (16), whereby any change in the level information signal is seen delayed from the viewpoint of the second transistor (33).

6. Switched mode power supply as defined in claim 4 or 5, c h a r a c t e r i z e d in that the delay element comprises an RC low pass filter (222, 223).

7. Switched mode power supply as defined in claim 1 or 2, c h a r a c t e r i z e d in that the controlled switch (24) is a FET transistor.

8. Switched mode power supply as defined in claim 1 or 2, c h a r a c t e r i z e d in that the controlled switch (24) is a bipolar transistor.


POWER ALARM
16
VOLTAGE MONITORING
U_{REF}
D3
-5V
- 5 V
10
12
U_{REF}
UNDER-VOLTAGE DETECTOR
N3
Cout3
D1
+ 5 V
+
Uin
-
R1
A
N1
Cout1
D2
+ 3,3 V
P
D1
13
Vc
Ck
C1
B
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15
14

FIG. 1

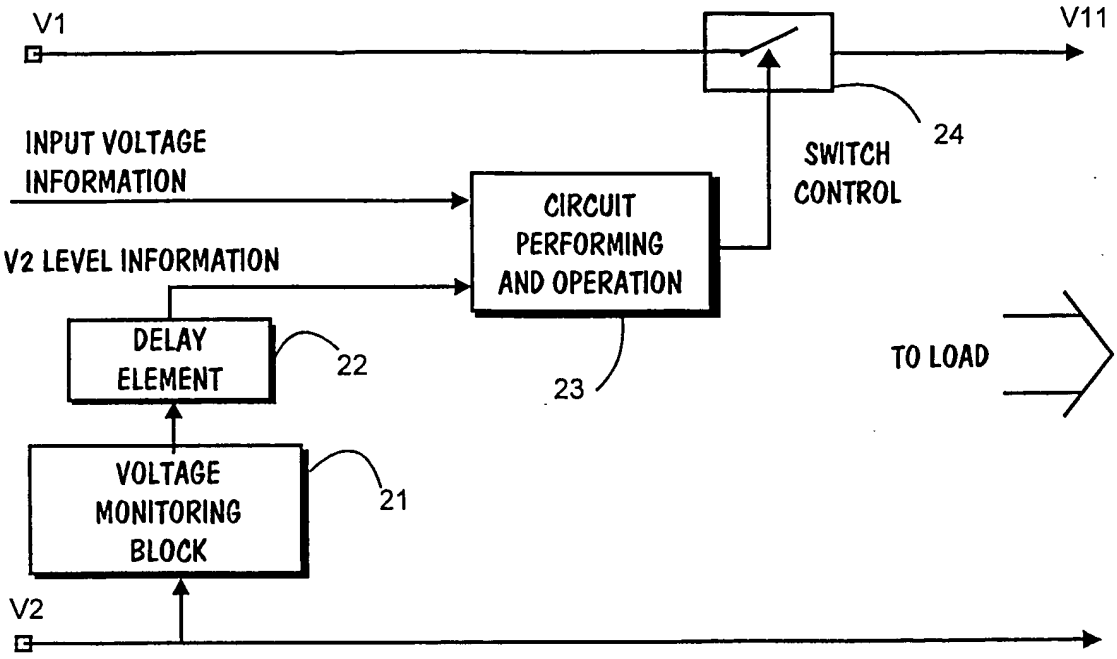


Fig. 2

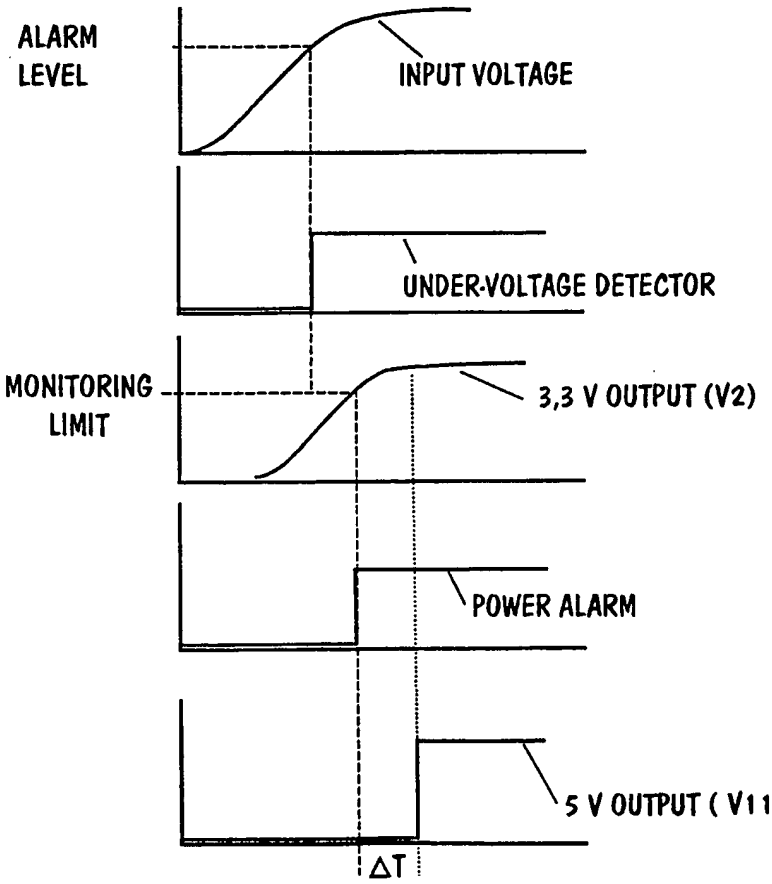


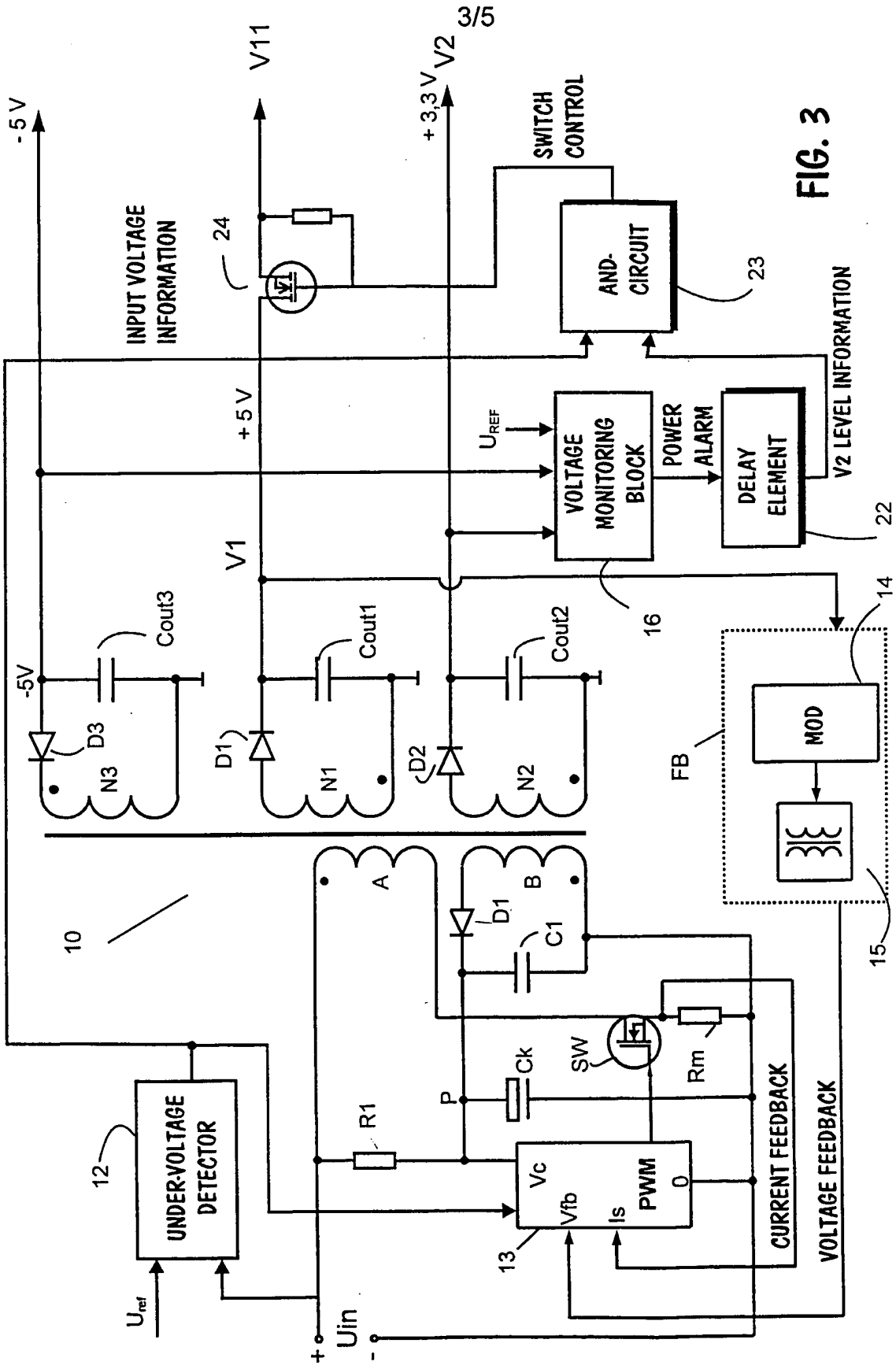
Fig. 4A

Fig. 4B

Fig. 4C

Fig. 4D

Fig. 4E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V11
+ 3,3 V
V2
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VOLTAGE MONITORING BLOCK
POWER ALARM
DELAY ELEMENT
V2 LEVEL INFORMATION
22
V1
16
14
Cout3
Cout1
Cout2
-5V
D3
D1
D2
N3
N1
N2
FB
MOD
10
A
B
D1
C1
15
SW
Rm
Ck
P
R1
12
UNDER-VOLTAGE DETECTOR
Vc
Vfb
Is
PWM
0
13
CURRENT FEEDBACK
VOLTAGE FEEDBACK
U_{ref}
Uin
+
-

FIG. 3

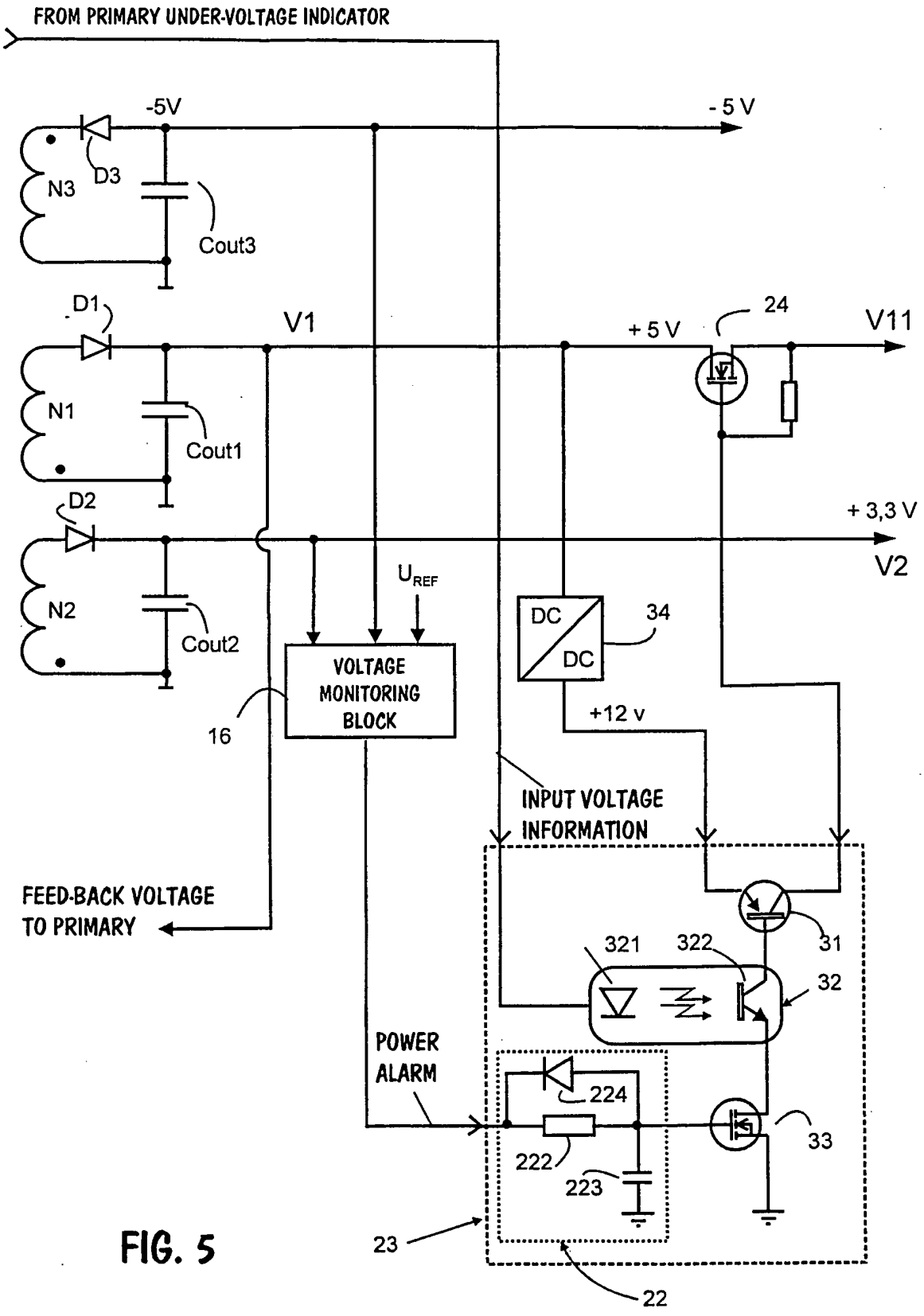
FROM PRIMARY UNDER-VOLTAGE INDICATOR
-5V
- 5 V
D3
N3
Cout3
D1
V1
+ 5 V
24
V11
N1
Cout1
D2
+ 3,3 V
V2
N2
Cout2
U_{REF}
DC
DC
34
VOLTAGE MONITORING BLOCK
16
+12 v
INPUT VOLTAGE INFORMATION
FEED-BACK VOLTAGE TO PRIMARY
321
322
31
32
POWER ALARM
224
222
223
33
23
22

FIG. 5

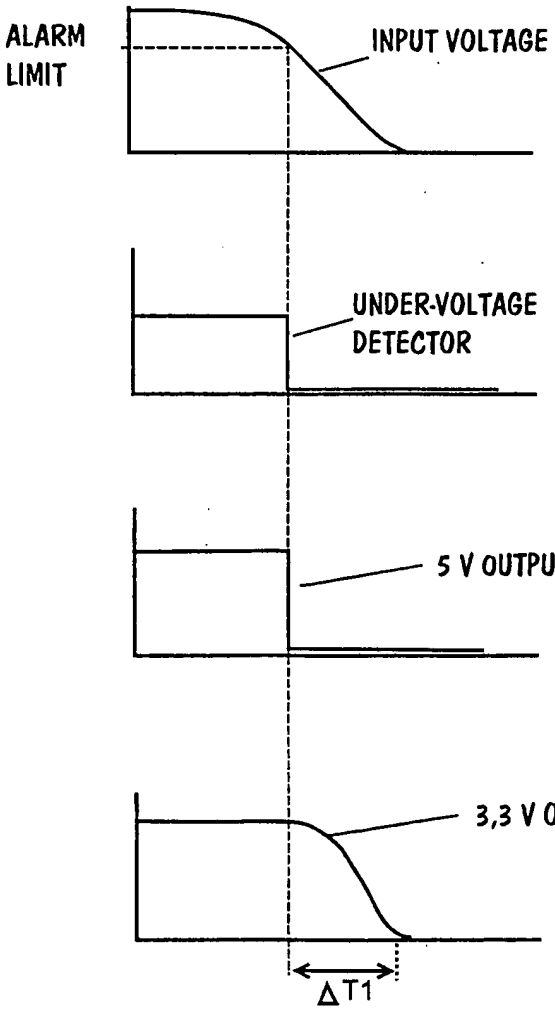

Fig. 6A

Fig. 6B

Fig. 6C

Fig. 6D